REMARKS

This is in full and timely response to the Final Office Action mailed on April 7, 2003. Reexamination in light of the amendments and the following remarks is respectfully requested.

Claims 2, 7-11, 13, and 15-20 are currently pending in this application, with claims 2, 7, 8 and 13 being independent.

Claims 7-8 and 15-20 have been withdrawn from consideration by the Examiner. A Petition Under 37 C.F.R. § 1.144 has been previously filed. Please timely consider this petition in light of the above-identified Final Office Action.

This amendment *prima facie* places the case in condition for allowance. Alternatively, it places this case in better condition for appeal. Accordingly, entry of this amendment is respectfully requested. No new matter is added.

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office action, respectfully requests reconsideration of the finality of the Office action for the reasons set forth hereinbelow. See M.P.E.P 706.07(c).

Drawings

Figure 1 has been amended within the previously filed

Request for Approval of Drawing Corrections, as requested by the Examiner. Withdrawal of the objection to the drawings is respectfully requested.

Rejections under 35 U.S.C. 112

Claims 9 and 12 were rejected under 35 U.S.C. 112, second paragraph.

This rejection is traversed at least for the following reasons.

While not conceding the propriety of this rejection and in order to advance the prosecution of this application, claim 9 has been amended and claim 12 has been canceled. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Rejections under 35 U.S.C. §102 and §103:

Claims 2, 10, 11 were rejected under 35 U.S.C. §102 as being allegedly anticipated by U.S. Patent No. 5,291,062 issued to Higgins, III (Higgins).

Claims 4, 9, 12-14 were rejected under 35 U.S.C. §103 as being allegedly obvious over Higgins.

These rejections are respectfully traversed for at least the

following reasons.

While not conceding the propriety of this rejection and in order to advance prosecution of the above-identified application, claims 4, 12 and 14 have been canceled, rendering this rejection moot as to claims 4, 12 and 14.

Claims 9-11 are dependent upon claim 2. Claim 2 is drawn to a semiconductor package comprising:

> a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;
>
> a sidewall section formed upright around said mounting portion of said first insulating substrate;
>
> a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and
>
> a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically

conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

wherein a heat radiating plate is provided on an opposite surface of said first insulating substrate.

Higgins is arguably teaches an area array semiconductor device having a lid with functional contacts.

The Office Action contends that Higgins teaches a first insulating substrate 42, 114. In this regard, a substrate 42 is found within figure 4, while a substrate 114 is found within figure 7.

However, note that Higgins fails to teach substrate 114 as an insulating substrate. Instead, Higgins arguably teaches that Substrate 114 has metallization 114 in the die cavity 106 to allow a plurality of semiconductor dice 102 to be interconnected, wherein the metallization 114 can be routed to different conductor planes in the substrate so that the dice do not have to be interconnected in-line, using the same bonding pads (column 8,

lines 19-25).

Higgins arguably teaches a cavity 16 within figure 4 and a cavity 106 within figure 7. However, Higgins fails to disclose, teach or suggest cavities 16, 106 being encapsulated by encapsulating resin, as claimed. Higgins is silent as to this feature and the Office Action fails to provide guidance as to where this feature is actually found.

Figures 4 and 7 of Higgins fails to disclose, teach or suggest a heat radiating plate is provided on an opposite surface of said first insulating substrate. In this regard, no heat radiating plate is shown within figures 4 and 7.

Claim 10 provides that the encapsulating resin is planarized. However, Higgins fails to disclose, teach or suggest a planarized encapsulating resin, wherein a cavity is encapsulated by the encapsulating resin, as claimed.

All features are not found within Higgins. Thus, Higgins fails to anticipate the claimed invention. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Claim 13, previously dependent upon claim 4, has been placed into independent form. Claim 13 is drawn to a semiconductor

package comprising:

a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

wherein said second insulating substrate is a laminated sheet lined on one side with copper, and

wherein said encapsulating resin is planarized.

The Office Action contends that Higgins teaches a first insulating substrate 42, 114. In this regard, a substrate 42 is found within figure 4, while a substrate 114 is found within figure 7.

However, note that Higgins fails to teach substrate 114 as an insulating substrate. Instead, Higgins arguably teaches that Substrate 114 has metallization 114 in the die cavity 106 to allow a plurality of semiconductor dice 102 to be interconnected, wherein the metallization 114 can be routed to different conductor planes in the substrate so that the dice do not have to be interconnected in-line, using the same bonding pads (column 8, lines 19-25).

Higgins arguably teaches a cavity 16 within figure 4 and a cavity 106 within figure 7. However, Higgins fails to disclose, teach or suggest cavities 16, 106 being encapsulated by encapsulating resin, as claimed. Higgins is silent as to this feature and the Office Action fails to provide guidance as to where this feature is actually found.

Higgins also fails to disclose, teach or suggest an encapsulating resin as being planarized.

Thus, Higgins fails to disclose, teach or suggest the claimed invention. Withdrawal of this rejection and allowance of the claims is respectfully requested.

New non-final Office Action

If the allowance of the claims is not forthcoming at the very least, then a **new non-final Office Action** is respectfully requested at least for the reasons provided hereinbelow.

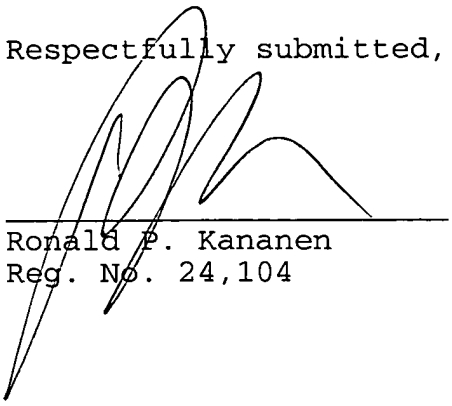
Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753, or the undersigned attorney at the below-listed number.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Respectfully submitted,



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APPENDIX

IN THE CLAIMS

Please cancel claims 4, 12 and 14 without prejudice or disclaimer of their underlying subject matter.

Please amend the claims as follows.

1. (canceled).

2. A semiconductor package comprising:

a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

wherein a heat radiating plate is provided on an opposite surface of said first insulating substrate.

3-6. (canceled).

7. A method for the preparation of a semiconductor package comprising the steps of:

forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate;

layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate;

mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer;

encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion;

layering a second insulating substrate carrying the a second electrically conductive pattern on one surface thereof on said spacer;

forming a through-hole for establishing electrical connection between said first electrically conductive pattern and said second electrically conductive pattern; and

forming solder lands at least on said cavity on said electrically conductive pattern,

wherein said second insulating substrate is a laminated sheet lined on one side with copper.

8. A method for the preparation of a semiconductor package comprising the steps of:

forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate;

layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate;

mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer;

encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion;

layering a second insulating substrate carrying the a second electrically conductive pattern on one surface thereof on said spacer;

forming a through-hole for establishing electrical connection between said first electrically conductive pattern and said second electrically conductive pattern;

forming solder lands at least on said cavity on said electrically conductive pattern; and

providing a heat radiating plate on the opposite surface of said first insulating substrate after forming said second electrically conductive pattern.

9. (amended) The semiconductor package according to claim 2, wherein said first insulating substrate is a laminated sheet lined ~~on both sides of the insulating substrate~~ with copper on said one surface and on said opposite surface.

10. The semiconductor package according to claim 2, wherein said encapsulating resin is planarized.

11. The semiconductor package according to claim 2, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection

of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

12. (amended) The semiconductor package according to claim 4, wherein said first insulating substrate is a laminated sheet lined ~~on both sides of the insulating substrate~~ with copper on said one surface and on said opposite surface.

13. (amended) A semiconductor package comprising:

a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

wherein said second insulating substrate is a laminated sheet lined on one side with copper~~The semiconductor package according to claim 4~~,

wherein said encapsulating resin is planarized.

14. The semiconductor package according to claim 4, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and

other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

15. The method according to claim 7, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

16. The method according to claim 7, wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

17. The method according to claim 7, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and

other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

18. The method according to claim 8, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

19. The method according to claim 8, wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

20. The method according to claim 8, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and

other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.